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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/785,268	02/24/2004	Dong-Hun Lee	8054-46 (AW8136US/MJ	3865

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EXAMINER	
LINDSAY JR, WALTER LEE	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 05/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

SM

Office Action Summary	Application No.	Applicant(s)	
	10/785,268	LEE ET AL.	
	Examiner	Art Unit	
	Walter L. Lindsay, Jr.	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *16-21* is/are allowed.

6)☒ Claim(s) *1,2,4,5,9 and 11* is/are rejected.

7)☒ Claim(s) *3,6-8,10 and 12-15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/9/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to an Application filed on 3/12/2003.

Currently, claims 1-21 are pending.

Specification

1. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2, 4-5, 9 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee et al. (U.S. Patent No. 5,872,047 dated 2/16/1999).

Lee shows the method as claimed in Figs. 2A-2D and corresponding text as: forming an N type gate pattern and a P type gate pattern on an N type transistor area (13) and a P type transistor area (15), respectively, of a semiconductor substrate (11) (Fig. 2A) (col. 3, lines 35-48); selectively implanting N type impurities (25) into the N type transistor area (col. 3, lines 35-48); forming an insulation layer (27) on the substrate including the N type gate pattern and the P type gate pattern (col. 3, lines 49-65); forming a first spacer (27) on sidewalls of the P type gate pattern by anisotropically etching a portion of the insulation layer in the P type transistor area while a portion of

the insulation layer (29) remains in the N type transistor area (col. 3, lines 49-65); and selectively implanting P type impurities (40B) into the P type gate pattern including the first spacer and into the P type transistor area (col. 4, lines 11-30) (claim 1). Lee teaches that the N type gate pattern and the P type gate pattern include a gate oxide layer pattern (19) and an undoped polysilicon layer pattern (21) (col. 3, lines 35-48) (claim 2). Lee teaches that a photoresist pattern (23) is formed on the substrate to selectively expose the N type transistor area; forming an N type impurity region having a low impurity concentration and an N type conductive gate pattern by implanting the N type impurities into the N type gate pattern and into the N type transistor area using the photoresist pattern as a mask (col. 3, lines 35-48); and removing the photoresist (col. 3, lines 49-65) (claim 4). Lee teaches that a photoresist pattern is formed on the substrate to selectively expose the P type transistor area, wherein forming the first spacer on the sidewall of the P type gate pattern by anisotropically etching the portion of the insulation layer in the P type transistor area includes using the photoresist pattern as an etching mask (col. 3, lines 35-48) (claim 9). Lee teaches that the N type impurities include arsenic (As) (25)(col. 3, lines 35-48)(claim 5). Lee teaches that the P type impurities (40B) include boron (B) (col. 4, lines 7-10) (claim 11).

Allowable Subject Matter

4. Claims 3, 6-8, 10, and 12-15 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. Claims 16-21 are allowed.

6. The following is a statement of reasons for the indication of allowable subject matter: the prior art, either singly or in combination fails to anticipate or render obvious, the limitations of:

...forming an oxide layer on the substrate including the N type gate pattern and the P type gate pattern to repair damage to the substrate and the gate patterns after forming the N type gate pattern and the P type gate pattern, as required by claim 3 as it depends on claim 1;

...selectively removing the portion of the insulation layer in the N type transistor region and selectively removing the first spacer on the P type transistor region, as required by claim 12 as it depends on claim 1; and

...forming a thermal oxidized layer on the substrate including the gate patterns to repair damage to the substrate and the gate patterns;

selectively implanting N type impurities into the N type gate patterns and into a portion of the substrate adjacent to the N type gate pattern to change the undoped polysilicon layer pattern into a conductive polysilicon layer and to form an N type impurity region having a low impurity concentration adjacent to the N type gate pattern; and

forming an insulation layer on the substrate including the gate patterns, as required by claim 16.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter L. Lindsay, Jr. whose telephone number is (571) 272-1674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Walter L. Lindsay, Jr.
Examiner
Art Unit 2812

WLL
April 29, 2005